WHAT IS CLAIMED:

1. A system comprising:

a plurality of processors implemented on at least two circuit boards;

a plurality of receiver/driver circuits each connected to a serial port of one of the plurality of processors;

a master processor coupled to the receiver/driver circuits to select one of the plurality of processors as an active processor for communicating diagnostic information to the master processor by instructing the receiver/driver circuit associated with the selected processor to logically connect the selected processor to the master processor; and

a bus connecting the master processor to the receiver/driver circuits.

2. The system of claim 1, wherein each of the plurality of processors is a control processor for one of the circuit boards.

3. The system of claim 2, wherein the circuit boards are each inserted into a physical housing.

4. The system of claim 3, wherein the bus is implemented in the physical housing.

5. The system of claim 4, wherein the circuit boards each perform functional operations in a network router.

6. The system of claim 1, further including:

control logic connected to the master processor and the receiver/driver circuits, the control logic activating, based on commands from the master processor, the selected one of the receiver/driver circuits and deactivating non-selected ones of the receiver/driver circuits.

7. The system of claim 6, wherein the non-selected ones of the receiver/driver circuits present high-impedance states to the bus.

8. The system of claim 1, further including:

an additional receiver/driver circuit connecting the master processor to the bus.

9. The system of claim 8, wherein the plurality of receiver/driver circuits and the additional receiver/driver circuit communicate using TTL signals.

10. The system of claim 9, further including:

a signal converter connected between the additional receiver/driver circuit and the master processor, the signal converter converting TTL signals for the additional receiver/driver circuit to RS-232 signals for the master processor.

11. The system of claim 1, further including:

a memory connected to each of the plurality of processors and storing boot code for initially bringing each of the plurality of processors on-line, the boot code permitting each of the plurality of processors to transmit diagnostic information before the boot code is fully loaded.

12. A method of obtaining diagnostic information from at least one of a plurality of processors in an electrical system, the method comprising:

receiving a request to receive diagnostic information from one of the plurality of processors;

connecting the selected processor to a bus;

electrically insulating non-selected processors of the plurality of processors from the bus; and

receiving the diagnostic information from the selected processor via a serial communication session transmitted over the bus; wherein

the selected processor being brought on-line by executing boot code, the boot code causing the selected processor to transmit the diagnostic information before the boot code is fully loaded.

13. The method of claim 12, wherein the serial communication session over the bus is implemented using TTL logic signals.

14. The method of claim 13, wherein each of the plurality of processors are located on a different circuit board.

15. The method of claim 14, wherein the bus is implemented in a physical housing of a network device.

16. A network device comprising:

a bus;

a packet forwarding engine having a plurality of circuit boards each including at least one processor and a receiver/driver circuit associated with each of the processors; and

a routing engine, connected to the bus, including a master processor, the master processor selecting one of the processors as an active processor for communicating diagnostic information by instructing the receiver/driver circuit associated with the selected processor to logically connect the selected processor to the bus.

17. The network device of claim 16, wherein the bus is implemented in a physical housing of the network device.

18. The network device of claim 16, wherein each of the processors is a control processor for the circuit board associated with the processor.

19. The network device of claim 17, wherein the circuit boards are each inserted into the physical housing.

20. The network device of claim 16, further including:

control logic connected to the master processor and the receiver/driver circuits, the control logic activating, based on commands from the master processor, the selected one of the receiver/driver circuits and deactivating non-selected ones of the receiver/driver circuits.

21. The network device of claim 20, wherein the non-selected ones of the receiver/driver circuits present high-impedance states to the bus.

22. The network device of claim 16, further including:

an additional receiver/driver circuit connecting the master processor to the bus.

23. The network device of claim 22, wherein the plurality of receiver/driver circuits and the additional receiver/driver circuit communicate using TTL signals.

24. The network device of claim 23, further including:

a signal converter connected between the additional receiver/driver circuit and the master processor, the signal converter converting TTL signals for the additional receiver/driver circuit to RS-232 signals for the master processor.

25. The network device of claim 16, further including:

memory connected to each of the plurality of processors and storing boot code for initially bringing each of the plurality of processors on-line, the boot code permitting each of the plurality of processors to transmit diagnostic information before the boot code is fully loaded.